

TITLE OF THE INVENTION
ON-CHIP LOOP FILTER FOR A PLL

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BACKGROUND OF THE INVENTION

TECHNICAL FIELD OF THE INVENTION

10 This invention relates generally to wireless communication devices and more particularly to phase locked loops.

DESCRIPTION OF RELATED ART

15 CMOS (complimentary metal oxide semiconductor) technology has enabled the integration of very complex circuitry into very small integrated circuit packages. However, some components must remain off-chip due to the precision needed, value flexibility needed, and/or the excessive die area required to implement the component on-chip. For instance, components of a loop filter of a local oscillation generator (which includes a phase locked loop) used in radio frequency integrated circuits by both the
20 transmit and receive sections are off-chip. While the off-chip components allow for greater flexibility in value selection, greater precision, and/or die area savings, it comes at the cost of pin count and increased noise.

25 As is known, at radio frequency (RF) frequencies (e.g., in the gigahertz), coupling between integrated circuits and external components via pins and board traces adds unwanted parasitics (e.g., inductance and capacitance) to the loop filter that adversely effect the performance of the local oscillation generator and hence adverse effects the overall performance of the radio frequency integrated circuit.

Therefore, a need exists for an on-chip loop filter for use within a local oscillation generator that provides similar advantages as off-chip components and minimizes the disadvantages.

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BRIEF SUMMARY OF THE INVENTION

The on-chip loop filter for a phase locked loop (PLL) of the present invention substantially meets these needs and others. In one embodiment, an on-chip loop filter includes a 1st resistor, a 1st capacitor, a 2nd capacitor, a 3rd capacitor, a 2nd resistor, and a 10 4th capacitor. The 1st resistor is operably coupled to receive a charge pump output. The 1st capacitor is coupled in series with the 1st resistor where the second node of the 1st capacitor is coupled to a return. The 2nd capacitor is coupled in parallel with the series combination of the 1st resistor and 1st capacitor. The 3rd capacitor is coupled in parallel with the 2nd capacitor. The 2nd resistor is coupled to a node of the 3rd capacitor and to a 15 node of the 4th capacitor. The other node of the 4th capacitor is coupled to ground. To enable these components to be placed on-chip, the 1st capacitor is of a 1st capacitor construct having a 1st quality factor, the 2nd capacitor is of a 2nd capacitor construct having a 2nd quality factor, where the 2nd quality factor is greater than the 1st quality factor, and the 3rd and 4th capacitors are of a 3rd capacitor construct having a 3rd quality 20 factor, which is greater than the 2nd quality factor. For example, the 3rd and 4th capacitors may be metal capacitors, the 2nd capacitor may be one or more narrow channel transistor capacitors, and the 1st capacitor may be one or more wide channel transistor capacitors. By creating an on-chip loop filter for a phase locked loop, which may be used in a local oscillation generator, the pin requirement for a radio frequency integrated circuit is 25 reduced as well as the corresponding noise for interfacing with external components.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Figure 1 is a schematic block diagram of a wireless communication system in 30 accordance with the present invention;

Figure 2 is a schematic block diagram of a wireless communication device in accordance with the present invention;

Figure 3 is a schematic block diagram of a local oscillation module in accordance
5 with the present invention;

Figure 4 is a schematic block diagram of a phase locked loop in accordance with the present invention;

10 Figure 5 is a schematic block diagram of an on-chip loop filter in accordance with the present invention;

Figure 6 is a geometric representation of a 1st construct capacitor in accordance with the present invention;

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Figure 7 is a graphical representation of a 2nd capacitor construct in accordance with the present invention; and

Figure 8 is a graphical representation of a 3rd capacitor construct in accordance
20 with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 is a schematic block diagram illustrating a communication system 10 that
25 includes a plurality of base stations and/or access points 12-16, a plurality of wireless communication devices 18-32 and a network hardware component 34. The wireless communication devices 18-32 may be laptop host computers 18 and 26, personal digital assistant hosts 20 and 30, personal computer hosts 24 and 32 and/or cellular telephone hosts 22 and 28. The details of the wireless communication devices will be described in
30 greater detail with reference to Figure 2.

The base stations or access points 12-16 are operably coupled to the network hardware 34 via local area network connections 36, 38 and 40. The network hardware 34, which may be a router, switch, bridge, modem, system controller, et cetera provides a wide area network connection 42 for the communication system 10. Each of the base stations or access points 12-16 has an associated antenna or antenna array to communicate with the wireless communication devices in its area. Typically, the wireless communication devices register with a particular base station or access point 12-14 to receive services from the communication system 10. For direct connections (i.e., point-to-point communications), wireless communication devices communicate directly via an allocated channel.

Typically, base stations are used for cellular telephone systems and like-type systems, while access points are used for in-home or in-building wireless networks. Regardless of the particular type of communication system, each wireless communication device includes a built-in radio and/or is coupled to a radio. The radio includes a highly linear amplifier and/or programmable multi-stage amplifier as disclosed herein to enhance performance, reduce costs, reduce size, and/or enhance broadband applications.

Figure 2 is a schematic block diagram illustrating a wireless communication device that includes the host device 18-32 and an associated radio 60. For cellular telephone hosts, the radio 60 is a built-in component. For personal digital assistants hosts, laptop hosts, and/or personal computer hosts, the radio 60 may be built-in or an externally coupled component.

As illustrated, the host device 18-32 includes a processing module 50, memory 52, radio interface 54, input interface 58 and output interface 56. The processing module 50 and memory 52 execute the corresponding instructions that are typically done by the host device. For example, for a cellular telephone host device, the processing module 50 performs the corresponding communication functions in accordance with a particular cellular telephone standard.

The radio interface 54 allows data to be received from and sent to the radio 60. For data received from the radio 60 (e.g., inbound data), the radio interface 54 provides the data to the processing module 50 for further processing and/or routing to the output interface 56. The output interface 56 provides connectivity to an output display device
5 such as a display, monitor, speakers, et cetera such that the received data may be displayed. The radio interface 54 also provides data from the processing module 50 to the radio 60. The processing module 50 may receive the outbound data from an input device such as a keyboard, keypad, microphone, et cetera via the input interface 58 or generate the data itself. For data received via the input interface 58, the processing
10 module 50 may perform a corresponding host function on the data and/or route it to the radio 60 via the radio interface 54.

Radio 60 includes a host interface 62, digital receiver processing module 64, an analog-to-digital converter 66, a filtering/gain module 68, an IF mixing down conversion
15 stage 70, a receiver filter 71, a low noise amplifier 72, a transmitter/receiver switch 73, a local oscillation module 74, memory 75, a digital transmitter processing module 76, a digital-to-analog converter 78, a filtering/gain module 80, an IF mixing up conversion stage 82, a power amplifier 84, a transmitter filter module 85, and an antenna 86. The antenna 86 may be a single antenna that is shared by the transmit and receive paths as
20 regulated by the Tx/Rx switch 73, or may include separate antennas for the transmit path and receive path. The antenna implementation will depend on the particular standard to which the wireless communication device is compliant.

The digital receiver processing module 64 and the digital transmitter processing
25 module 76, in combination with operational instructions stored in memory 75, execute digital receiver functions and digital transmitter functions, respectively. The digital receiver functions include, but are not limited to, digital intermediate frequency to baseband conversion, demodulation, constellation demapping, decoding, and/or descrambling. The digital transmitter functions include, but are not limited to,
30 scrambling, encoding, constellation mapping, modulation, and/or digital baseband to IF conversion. The digital receiver and transmitter processing modules 64 and 76 may be

implemented using a shared processing device, individual processing devices, or a plurality of processing devices. Such a processing device may be a microprocessor, micro-controller, digital signal processor, microcomputer, central processing unit, field programmable gate array, programmable logic device, state machine, logic circuitry, analog circuitry, digital circuitry, and/or any device that manipulates signals (analog and/or digital) based on operational instructions. The memory 75 may be a single memory device or a plurality of memory devices. Such a memory device may be a read-only memory, random access memory, volatile memory, non-volatile memory, static memory, dynamic memory, flash memory, and/or any device that stores digital information. Note that when the processing module 64 and/or 76 implements one or more of its functions via a state machine, analog circuitry, digital circuitry, and/or logic circuitry, the memory storing the corresponding operational instructions is embedded with the circuitry comprising the state machine, analog circuitry, digital circuitry, and/or logic circuitry.

In operation, the radio 60 receives outbound data 94 from the host device via the host interface 62. The host interface 62 routes the outbound data 94 to the digital transmitter processing module 76, which processes the outbound data 94 in accordance with a particular wireless communication standard (e.g., IEEE 802.11 Bluetooth, et cetera) to produce digital transmission formatted data 96. The digital transmission formatted data 96 will be a digital base-band signal or a digital low IF signal, where the low IF typically will be in the frequency range of one hundred kilohertz to a few megahertz.

The digital-to-analog converter 78 converts the digital transmission formatted data 96 from the digital domain to the analog domain. The filtering/gain module 80 filters and/or adjusts the gain of the analog signal prior to providing it to the IF mixing stage 82. The IF mixing stage 82 converts the analog baseband or low IF signal into an RF signal based on a transmitter local oscillation 83 provided by local oscillation module 74. The power amplifier 84 amplifies the RF signal to produce outbound RF signal 98, which is filtered by the transmitter filter module 85. The antenna 86 transmits the

outbound RF signal 98 to a targeted device such as a base station, an access point and/or another wireless communication device.

The radio 60 also receives an inbound RF signal 88 via the antenna 86, which was
5 transmitted by a base station, an access point, or another wireless communication device. The antenna 86 provides the inbound RF signal 88 to the receiver filter module 71 via the Tx/Rx switch 73, where the Rx filter 71 bandpass filters the inbound RF signal 88. The Rx filter 71 provides the filtered RF signal to low noise amplifier 72, which amplifies the signal 88 to produce an amplified inbound RF signal. The low noise amplifier 72
10 provides the amplified inbound RF signal to the IF mixing module 70, which directly converts the amplified inbound RF signal into an inbound low IF signal or baseband signal based on a receiver local oscillation 81 provided by local oscillation module 74. The down conversion module 70 provides the inbound low IF signal or baseband signal to the filtering/gain module 68. The filtering/gain module 68 filters and/or gains the
15 inbound low IF signal or the inbound baseband signal to produce a filtered inbound signal.

The analog-to-digital converter 66 converts the filtered inbound signal from the analog domain to the digital domain to produce digital reception formatted data 90. The
20 digital receiver processing module 64 decodes, descrambles, demaps, and/or demodulates the digital reception formatted data 90 to recapture inbound data 92 in accordance with the particular wireless communication standard being implemented by radio 60. The host interface 62 provides the recaptured inbound data 92 to the host device 18-32 via the radio interface 54.

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As one of average skill in the art will appreciate, the wireless communication device of figure 2 may be implemented using one or more integrated circuits. For example, the host device may be implemented on one integrated circuit, the digital receiver processing module 64, the digital transmitter processing module 76 and memory
30 75 may be implemented on a second integrated circuit, and the remaining components of the radio 60, less the antenna 86, may be implemented on a third integrated circuit. As an

alternate example, the radio 60 may be implemented on a single integrated circuit. As yet another example, the processing module 50 of the host device and the digital receiver and transmitter processing modules 64 and 76 may be a common processing device implemented on a single integrated circuit. Further, the memory 52 and memory 75 may
5 be implemented on a single integrated circuit and/or on the same integrated circuit as the common processing modules of processing module 50 and the digital receiver and transmitter processing module 64 and 76.

Figure 3 is a schematic block diagram of a local oscillation module 74 that
10 includes a phase locked loop 100, a divide-by-two module 102, a summation module 103 and two output buffers 105 and 107. The phase locked loop 100 receives a reference oscillation 104 that it converts into an output oscillation 122. The reference oscillation 124 may be generated by a crystal oscillator that produces a 10-25 megahertz signal. The frequency of the output oscillation 122 is dependent on the desired frequency of the
15 transmit local oscillation 83 and the receive local oscillation 81. For example, if the desired transmit and receive local oscillations 81 and 83 is 2.4 gigahertz, the output oscillation 122 will be 1.6 gigahertz (i.e., two-thirds of the desired local oscillation such that when it is summed with one-half of its frequency, i.e., one-third of the desired local oscillation, the resulting oscillation is at the desired rate).

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The divide-by-two module 102 divides the frequency of the output oscillation 122 by two. In the previous example, the divide-by-two module 102 will produce a clock signal having a frequency of 800 megahertz. The summation module 103 sums the output oscillation 122 with the output produced by the divide-by-two module 102 to
25 produce the desired local oscillation. For instance, with the 2.4 gigahertz local oscillation example, the output oscillation 122 has a frequency of 1.6 gigahertz, the output of the divide-by-two module has a frequency of 0.8 gigahertz, when summed together the 2.4 gigahertz is achieved. As one of average skill in the art will appreciate, the transmit local oscillation 83 on the receive local oscillation 81 may include an in-phase component and
30 a quadrature component.

Figure 4 is a schematic block diagram of a phase locked loop 100 that includes an oscillation comparator 106, a charge pump 108, a loop filter 110, a voltage controlled oscillator 112, and a feedback module 114. The oscillation comparator 106 may be a phase comparator or a phase and frequency comparator. The oscillation comparator 106 compares the phase and/or frequency differences between the reference oscillation 104 and a feedback oscillation 124. The feedback oscillation 124 is generated by the feedback module 114, which divides the frequency of the output oscillation 122 by a divider value. For example, if the reference oscillation 104 is a 20 megahertz signal and the output oscillation 122 is 1.6 gigahertz, the divider value will be 80, which produces a feedback oscillation 124 of 20 megahertz.

The charge pump 108 receives the difference signal 116 from the oscillation comparator 106 and generates a corresponding charge pump signal 118. In one embodiment, the charge pump 108 may be a current charge pump that produces a positive current when the frequency of the output oscillation 122 needs to be increased and/or the phase offset of the output oscillation 122, with respect to the reference oscillation, needs to be decreased. Conversely, if the output oscillation 122 has a leading phase or is at a too high of a frequency, the charge pump produces a negative current that slows the frequency of the output oscillation 122 and/or increases the phase offset of the output oscillation 122.

The loop filter 110 converts the charge pump signal 118 into a control voltage 120 that is provided to the voltage controlled oscillator 112. The voltage controlled oscillator 112, based on the control voltage 120, produces the output oscillation 122. For instance, as the control voltage increases, which it does so with a positive current charge pump signal 118, the frequency of the output oscillation increases and/or the phase offset decreases. Conversely, as the control voltage 120 decreases, the frequency of the output oscillation 122 decreases and the phase offset increases.

Figure 5 is a schematic block diagram of loop filter 110 that includes a 1st resistor (R1), a 1st capacitor (C1), a 2nd capacitor (C2), a 3rd capacitor (C3), a 2nd resistor (R2),

and a 4th capacitor (C4). The 1st capacitor C1 is of a 1st capacitor construct which is illustrated in Figure 8. As shown in Figure 8, the 1st capacitor construct is a wide channel transistor. To produce a capacitor from a transistor, the drain (D) is electrically coupled to the source (S) of the transistor. In this embodiment, the distance between the source and drain is relatively wide thus producing a relatively large capacitance value in a relatively small die area, however, the quality factor (Q) is relatively low. For instance, in one embodiment, the 1st capacitor may have a capacitance value of 2.2 nano farads (+ or – 20%) with a quality factor of approximately 30. Note that the 1st capacitor may include one or more wide channel transistors configured as a capacitor to achieve the desired capacitance. In furtherance of this example, resistor R1 may have a resistance value of 4.7 kilo-Ohms.

The 2nd capacitor C2 is of a 2nd capacitor construct as illustrated in Figure 7. The 2nd capacitor construct is a narrow channel transistor that includes a drain and source within a well, where the drain and source are relatively close to each other. This type of capacitor structure, when the drain and source are coupled together, produce a capacitor having a higher quality factor than that of the 1st capacitor construct (e.g., Q approximately 100) but also produces a smaller capacitance value per die area. In continuation with the example above, the 2nd capacitor may have a capacitance value of 150 pico-farads and may include one or more narrow channel transistors to achieve the desired capacitance value.

The 3rd and 4th capacitors are of the 3rd capacitor construct which is illustrated in Figure 6. As shown in Figure 6, the 3rd capacitor construct is a metal fringe, or finger, capacitor that includes metal plates fabricated on one or more metal layers of an integrated circuit. Such a capacitor produces precision capacitors (e.g., capacitance values having a tolerance of approximately 5%) and a high quality factor (Q approximately equal to 200) but consumes a relatively large die area per capacitance value. As such, it is desired that the capacitance value of the 3rd and 4th capacitors be relatively small. Continuing with the above example, the 3rd capacitor may have a capacitance value of 50 pico-farads and the 4th capacitor may have a capacitance value of

20 pico-farads. Continuing with this example, the 2nd resistor may have a resistance value of 200 Ohms.

To facilitate the desired noise immunity, the 2nd resistor R2 and the 4th capacitor C4 should be placed near the input of the voltage controlled oscillator 112. In addition, capacitor C2 and C3 may be stacked on top of each other on different metal layers. Further, resistors R1 and R2 and capacitors C1-C3 may have a ground plane underneath them to enhance shielding. Further, one or more of the resistors R1 and R2 may be variable as well as one or more of capacitors C1-C4. If variable components are used, an RC calibration circuit may be included to tune the values of the variable resistors and/or capacitors.

By placing R2 and C4 in layout near the inputs of the VCO, which may include on-chip inductors that have a relatively low quality factor (e.g., less than 20), the desired loop filtering is achieved on-chip. As such, the need for pins to couple to external components is eliminated as well as the associated noise produced as a result of the external coupling.

As one of average skill in the art will appreciate, the term “substantially” or “approximately”, as may be used herein, provides an industry-accepted tolerance to its corresponding term. Such an industry-accepted tolerance ranges from less than one percent to twenty percent and corresponds to, but is not limited to, component values, integrated circuit process variations, temperature variations, rise and fall times, and/or thermal noise. As one of average skill in the art will further appreciate, the term “operably coupled”, as may be used herein, includes direct coupling and indirect coupling via another component, element, circuit, or module where, for indirect coupling, the intervening component, element, circuit, or module does not modify the information of a signal but may adjust its current level, voltage level, and/or power level. As one of average skill in the art will also appreciate, inferred coupling (i.e., where one element is coupled to another element by inference) includes direct and indirect coupling between two elements in the same manner as “operably coupled”. As one of average skill in the

art will further appreciate, the term “compares favorably”, as may be used herein, indicates that a comparison between two or more elements, items, signals, etc., provides a desired relationship. For example, when the desired relationship is that signal 1 has a greater magnitude than signal 2, a favorable comparison may be achieved when the
5 magnitude of signal 1 is greater than that of signal 2 or when the magnitude of signal 2 is less than that of signal 1.

The preceding discussion has presented an on-chip loop filter for use within a phase locked loop, which in turn may be used within a local oscillation generator. By
10 implementing an on-chip loop filter, the adverse effects of external components is substantially reduced while with the varied construct of the loop filter, the advantages are substantially maintained. As one of average skill in the art will appreciate, other embodiments may be derived from the teaching of the present invention without deviating from the scope of the claims.

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